Claims

1. An integrated circuit semiconductor memory device (100) comprising:

a substrate (112);

a first dielectric layer (116) covering a first portion (114a) of said substrate, said first dielectric layer being absent from a second portion (130) of said substrate;

a second dielectric layer (132) having a property different from said first dielectric layer, said second dielectric layer at least partly covering said second portion (130) of said substrate;

a source region (118) formed in a first doped region on said first dielectric layer;

a drain region (120) formed in a second doped region on said first dielectric layer; and

a gate (128) formed over said second dielectric layer and between said first and second doped regions,

wherein said property of said second dielectric layer provides a gate capacitance of said gate with respect to said substrate that is greater than a theoretical capacitance of a gate formed over said first dielectric layer on said substrate.

2. The device of claim 1, wherein said device is RAM.

3. The device of claim 1, wherein said device is SRAM.

4. The device of claim 1, wherein said device includes a FET.

5. The device of claim 4, wherein said FET is a FinFET.

6. The device of claim 1 or claim 5, wherein said first dielectric layer is a buried oxide layer (116) and said second dielectric layer is a thin oxide layer (132) providing less insulating effect than said buried oxide layer, said gate being capacitively coupled to said substrate.

7. The device of claim 6, wherein a fin (122) of said FinFET is formed

over said buried oxide layer.

8. The device of claim 1 or claim 5, wherein said device further comprises a fin (122) and a gate dielectric layer (124, 126) between said gate and said fin, wherein said second dielectric layer has less leakage than said gate dielectric layer.

9. The device of claim 1 or claim 5, wherein said substrate has an upwardly-facing first surface (314a) at an upper level and an upwardly-facing second surface (314b) at a lower level, said first dielectric layer being a dielectric layer formed on said first surface, said second dielectric layer being a dielectric layer formed on said second surface, and a fin (322) of said FinFET is formed over said buried layer.

10. The device of claim 9, wherein said first dielectric layer is a buried oxide layer (316) and said second dielectric layer is a thin oxide layer (332a, 332b).

11. The device of claim 8, wherein said first dielectric layer is a buried oxide layer (116) and said second dielectric layer is a thin oxide layer (132).